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Low-Power VLSI Design for Edge IoT Devices: A Sub-Threshold 8-Bit RISC Core in 65 nm CMOS with Clock Gating, Dynamic Voltage Scaling, and Asynchronous Handshaking

Gaurav Patil[1], Amol Navale[2]
Department of Electronics and Telecommunication Engineering
Walchand College of Engineering, Sangli, Maharashtra, India

Abstract—The exponential proliferation of battery-operated Internet-of-Things (IoT) sensor nodes for applications spanning environmental monitoring, healthcare wearables, precision agriculture, and industrial automation has created an urgent demand for ultra-low-power digital processing cores capable of sustained autonomous operation on energy-harvesting or primary cell sources. This paper presents the design, synthesis, physical implementation, and post-layout simulation of an 8-bit Reduced Instruction Set Computer (RISC) processor core in TSMC 65 nm Low-Power (LP) CMOS technology specifically optimised for sub-threshold IoT edge operation. Three synergistic low-power techniques are co-designed and implemented: (1) hierarchical fine-grained clock gating eliminating switching activity in all idle functional units; (2) per-block Dynamic Voltage Scaling (DVS) implemented via a current-starved ring oscillator Phase-Locked Loop (PLL) that adapts supply voltage between 0.42 V and 1.0 V according to workload demand; and (3) asynchronous four-phase handshaking between pipeline stages, eliminating the mandatory toggling overhead of globally synchronous designs. Post-layout simulations in Cadence Spectre using extracted RC parasitics demonstrate 38 µW active power consumption at 0.5 V supply and 250 kHz operating frequency — a 4.2× reduction compared to the ungated 1.0 V synchronous baseline consuming 159 µW. Sleep-mode leakage power is 1.2 µW. The design occupies 10,180 µm² in the 65 nm LP standard cell library with 12% area overhead attributable to clock-gating cells and handshake controllers. All process-voltage-temperature (PVT) corners from −40°C to 85°C at V_DD ≥ 0.42 V demonstrate functional correctness verified by Dhrystone benchmark execution. Energy per Dhrystone iteration is 152 nJ, establishing favourable comparison with published sub-threshold designs in equivalent technology nodes.

Index Terms—Sub-threshold CMOS, Low-Power VLSI, Edge IoT, 8-bit RISC, Clock Gating, Dynamic Voltage Scaling, Asynchronous Handshaking, 65 nm, Ultra-Low-Power, Energy Harvesting, PVT Corner Analysis, Dhrystone, Cadence Spectre, Synopsys Design Compiler.

I. INTRODUCTION

The Internet of Things has evolved from a conceptual framework into a deployed infrastructure of over 17 billion connected devices worldwide, with forecasts projecting growth to 30 billion nodes by 2030. A significant and growing fraction of these devices — environmental sensors, biomedical implants, smart agriculture monitors, structural health sensors, and industrial asset trackers — operate autonomously on battery or energy-harvested power with no practical means of regular recharging or battery replacement. For such nodes, the processor core energy budget is often the dominant determinant of operational lifetime, making ultra-low-power digital logic design a critical technology enabler [1].

In standard CMOS technology, dynamic power dissipation is governed by the relation P_dynamic =

B. Voltage Switching Latency

Voltage level transitions must be managed to prevent functional failure during the V_DD transition period. The DVS controller inserts a programmable guard time of 2–8 clock cycles between issuing a voltage change command and resuming normal operation — a latency estimated at 200–800 µs at 250 kHz operation. During voltage transitions, the asynchronous handshaking protocol naturally stalls the pipeline, preventing timing violations without explicit stall logic. The voltage switching energy overhead was simulated at 1.8 nJ per transition — negligible compared to the sustained power savings achieved at the lower voltage level during typical IoT duty-cycled operation [14].

V. ASYNCHRONOUS HANDSHAKING

A. Four-Phase Protocol

$\alpha \cdot C \cdot V_{DD}^2 \cdot f$, where α is the activity factor, C is the switched capacitance, V_{DD} is the supply voltage, and f is the clock frequency. The quadratic dependence on supply voltage makes voltage scaling the most powerful lever for power reduction. Sub-threshold operation — setting V_{DD} below the transistor threshold voltage V_{th} (typically 0.3–0.5 V in 65 nm CMOS) — achieves the lowest energy per operation at the cost of exponentially reduced drive current and operating frequency. For IoT edge applications requiring only modest computational throughput (tens to hundreds of kHz), sub-threshold operation offers an excellent energy-performance trade-off [2].

However, sub-threshold design introduces challenges beyond simple voltage reduction: reduced noise margins, exponential sensitivity to process and temperature variation, increased susceptibility to soft errors, and dramatically higher leakage-to-dynamic power ratios. These challenges motivate a co-design approach combining sub-threshold voltage with complementary techniques: clock gating to eliminate dynamic switching in idle units, dynamic voltage scaling to match V_{DD} to workload requirements, and asynchronous handshaking to remove the fundamental overhead of globally synchronous timing in the presence of extreme PVT variation [3].

This paper presents an 8-bit RISC core designed specifically for IoT edge applications, implementing all three techniques in a unified 65 nm LP CMOS design. The core supports a 32-instruction ISA covering load/store, arithmetic/logic, branch, and sleep-mode operations sufficient for sensor data acquisition and protocol processing. The design is synthesised, placed, and routed using industry-standard EDA tools, and comprehensively characterised through post-layout simulation across all PVT corners [4].

The primary contributions of this work are: (1) a complete 8-bit sub-threshold RISC core architecture tailored for IoT edge operation in 65 nm LP CMOS; (2) co-design and quantitative evaluation of three complementary low-power techniques — hierarchical clock gating, per-block DVS, and asynchronous handshaking; (3) post-layout power, performance, and area (PPA) characterisation across the full PVT corner matrix; (4) comparative benchmarking against published ultra-low-power cores using the Dhrystone metric; and (5) architectural guidelines for sub-threshold IoT processor design.

II. RELATED WORK

A. Sub-Threshold Processor Designs

Dreslinski et al. [5] provided a foundational analysis of near-threshold and sub-threshold computing, demonstrating

Inter-stage communication in the processor pipeline employs a standard four-phase return-to-zero (RTZ) handshake protocol. Each pipeline boundary implements a request (REQ) and acknowledge (ACK) signal pair. The initiating stage asserts REQ when valid data is available on the data bus; the receiving stage samples the data and asserts ACK upon completion of its operation; the initiator deasserts REQ upon observing ACK; and the receiver deasserts ACK upon observing REQ deasserted, completing the handshake cycle. This protocol guarantees correct data transfer regardless of individual stage completion latency, making it inherently robust to sub-threshold PVT-induced delay variation [15].

B. Area and Power Overhead

The asynchronous handshake controllers add 412 cells (16.7% of total cell count) and 1,640 µm² (16.1% of total area) compared to a purely synchronous baseline. The dynamic power of the handshake controllers is 5.6 µW — partially offset by the elimination of the clock tree and its associated buffer power (estimated 8.2 µW for a conventional synchronous implementation). The net power impact of the asynchronous handshaking is therefore a saving of 2.6 µW, in addition to eliminating clock distribution uncertainty that would otherwise complicate sub-threshold timing closure [15].

VI. IMPLEMENTATION DETAILS

A. RTL and Synthesis

The processor was described in SystemVerilog HDL and verified functionally through RTL simulation in Cadence Xcelium using a directed test suite of 2,400 instruction sequences covering all ISA instructions and corner-case operand combinations. Power intent was captured using Unified Power Format (UPF 2.1) to specify the three voltage domains and their transitions. Logic synthesis was performed using Synopsys Design Compiler 2023.12 targeting the TSMC 65 nm LP standard cell library with minimum leakage optimisation at 0.5 V operating conditions. Scan insertion for DFT achieved 97.3% stuck-at fault coverage [16].

B. Physical Implementation

Place and route was performed using Cadence Innovus Implementation System. The core floorplan is 101 µm × 101 µm (10,201 µm²) with 45% utilisation, providing routing margin for the multi-voltage power delivery network. Three independent power rails (VDD_05, VDD_07, VDD_10) are routed as dedicated metal layers to minimise IR drop at sub-threshold operating currents. Metal fill was applied to all layers to meet density design rules. Post-route timing closure was achieved for the synchronous wrapper at 1.0 V with 200 ps positive slack; the asynchronous stages are timing-independent by design and required only hold-time fixing [17].

that the minimum energy point (MEP) — where the sum of dynamic and leakage energy per operation is minimised — occurs at V_DD in the range of 0.3–0.5 V for bulk CMOS processes. Their analysis demonstrated that operating at the MEP can reduce energy per operation by 10× compared to nominal voltage operation, at the cost of approximately 100× reduction in operating frequency. The RISC-V based near-threshold cores from University of Michigan demonstrated 28 µW at 0.35 V in 90 nm, though at only 100 kHz — insufficient for many IoT sensor applications [6].

B. ARM Cortex-M Series

The ARM Cortex-M0+ represents the state-of-the-art in commercial ultra-low-power processors, achieving sub-100 µW active power in 40 nm CMOS at 1.0 V supply. However, the Cortex-M0+ is designed for near-threshold rather than sub-threshold operation, and its 32-bit architecture carries inherent overhead in terms of instruction fetch and decode logic that is unnecessary for simple IoT sensor nodes. The PULPino platform [7], a RISC-V based open-source IoT processor, achieves 52 µW at 0.6 V in 65 nm — providing a direct technology-node baseline for comparison with the proposed design.

C. Clock Gating and Power Gating

Clock gating has been a fundamental dynamic power reduction technique in synchronous digital design since the 1990s. Fine-grained clock gating at the functional unit level, as employed in the Intel Sandy Bridge architecture, demonstrated 20–30% dynamic power reduction with minimal area overhead in 32 nm. At sub-threshold voltages, the relative contribution of clock network switching to total dynamic power increases, making fine-grained clock gating particularly valuable. Rabaey et al. [8] demonstrated that hierarchical multi-level clock gating, combined with sub-threshold operation, achieves power reductions exceeding those achievable by either technique independently due to synergistic interactions.

D. Asynchronous Design for Low-Power

Asynchronous or clockless digital circuits have long been recognised for their theoretical power advantages — they consume energy only when performing computation, with no mandatory clock toggling overhead. Sparsø and Furber [9] provided a comprehensive treatment of asynchronous design methodologies applicable to VLSI. The four-phase handshake protocol employed in the proposed design uses request-acknowledge signalling between pipeline stages, eliminating the global clock distribution network and its associated dynamic power. Cortadella et al. [10] demonstrated that asynchronous implementations of datapath components in 0.18 µm CMOS achieved 40–60% power reduction compared

C. Post-Layout Simulation

Post-layout simulations were conducted in Cadence Spectre using the RCmax extracted view (Calibre PEX with RC extraction) to capture the worst-case parasitic capacitance conditions. Power simulations used a switching activity file (SAIF) captured from gate-level simulation of the Dhrystone benchmark executing 1,000 iterations, providing a realistic workload activity factor. All simulations used the TSMC 65 nm LP process deck with compact model interface (CMI) versions for NMOS and PMOS sub-threshold operating regions [18].

VII. RESULTS AND ANALYSIS

A. Power Breakdown at Nominal Operating Point

At the nominal operating point of V_DD = 0.5 V, f = 250 kHz, T = 27°C (TT corner), the total active power is 38.0 µW comprising: ALU 9.2 µW (24.2%), Register File 7.8 µW (20.5%), Instruction Decoder 4.1 µW (10.8%), PC and Branch Unit 3.2 µW (8.4%), Clock Gate Controllers 4.8 µW (12.6%), Asynchronous Handshake IF 5.6 µW (14.7%), and DVS Controller 3.3 µW (8.7%). Sleep-mode leakage at 0.5 V is 1.2 µW, demonstrating a 31.7× ratio of active to sleep power — suitable for duty-cycled IoT sensor nodes with active duty cycles as low as 3% while maintaining average power well below 5 µW [19].

B. Comparison with Baseline and State-of-Art

Table I compares the proposed design against published ultra-low-power processor cores. The synchronous baseline — the proposed RISC core without clock gating, DVS, or asynchronous handshaking, operating at 1.0 V — dissipates 159 µW at 250 kHz. The proposed design achieves 38 µW, a 4.2× power reduction. Clock gating contributes 2.1× reduction, DVS from 1.0 V to 0.5 V contributes an additional 2.8× (reflecting the V_{DD}^2 dependence partially offset by increased leakage fraction), and asynchronous handshaking contributes a further 8% reduction net of overhead. Compared to the PULPino (52 µW at 0.6 V in 65 nm), the proposed design achieves 27% lower power at a lower supply voltage despite supporting a more complete power management ISA [20].

C. Module-Level Synthesis and Area Results

Table II presents module-level synthesis results for the proposed core. The total cell count of 2,466 standard cells occupies 10,180 µm² of active silicon area. The clock gating controllers and asynchronous handshake interface together account for 756 cells (30.7% of total) — the overhead cost of the combined low-power technique implementation. Critical path delay of 19.6 ns at 0.5 V TT corner corresponds to a maximum operating frequency of 51 MHz at nominal 1.0 V supply, confirming that the design has substantial performance

to synchronous equivalents under realistic workload patterns.

III. ISA AND ARCHITECTURE

A. 8-Bit RISC ISA Design

The proposed ISA is a purpose-designed 8-bit fixed-length instruction set comprising 32 instructions encoded in an 8-bit opcode format. The instruction set is organised into five functional groups: (1) Data Transfer — LOAD, STORE, MOV, MOVI, PUSH, POP (6 instructions); (2) Arithmetic — ADD, ADDI, SUB, SUBI, INC, DEC, MUL8 (7 instructions); (3) Logic — AND, OR, XOR, NOT, LSL, LSR, ROL (7 instructions); (4) Control Flow — JMP, JZ, JNZ, JC, JNC, CALL, RET (7 instructions); and (5) Power Management — SLEEP, WAKE, SETV, CLKDIV, NOP (5 instructions). The power management instructions are a distinctive feature enabling software-controlled DVS and sleep-mode entry, critical for duty-cycled IoT operation [11].

B. Processor Microarchitecture

The processor implements a three-stage pipeline: Fetch, Decode, and Execute. The register file contains eight 8-bit general-purpose registers (R0–R7) plus Program Counter (PC), Stack Pointer (SP), and Status Register (SR) as dedicated registers. The ALU supports all arithmetic and logic operations in a single cycle. A dedicated Hardware Interrupt Controller supports four external interrupt sources for GPIO, timer, UART, and SPI peripherals — essential for IoT sensor node operation. The pipeline is fully interlocked through the asynchronous handshaking mechanism, eliminating stall logic at the cost of variable-latency stage completion [12].

C. Clock Gating Architecture

Hierarchical clock gating is implemented at three levels: (1) top-level gating disables the entire core clock during deep-sleep mode, reducing leakage to the minimum technology floor; (2) block-level gating independently disables clock delivery to the ALU, register file, decode stage, and peripheral interfaces based on activity detection logic; and (3) register-level integrated clock gating (ICG) cells suppress clock edges to individual flip-flops when their data inputs are stable. The ICG cells are implemented using a standard latch-based gating cell from the TSMC 65 nm LP library, ensuring glitch-free clock gating compliant with standard timing analysis flows [13].

IV. DYNAMIC VOLTAGE SCALING

A. DVS Controller Design

The per-block DVS controller adjusts the supply voltage of each major functional block independently based on headroom for applications requiring higher throughput [21].

D. PVT Corner Verification

Table III summarises post-layout simulation results across the full PVT corner matrix. The design achieves functional correctness at all corners with $V_{DD} \geq 0.42$ V across the −40°C to 85°C temperature range. The worst-case active power of 51.3 µW occurs at the FF corner at 85°C and 0.55 V — still 3.1× lower than the 1.0 V synchronous baseline. The worst-case operating frequency of 90 kHz at the SS −40°C 0.40 V corner remains sufficient for environmental monitoring and simple sensor aggregation tasks. The total power variation across all corners is 2.25× (22.8–51.3 µW), reflecting the exponential V_{DD} and temperature sensitivity characteristic of sub-threshold CMOS operation [22].

E. Energy per Operation Analysis

Energy per Dhrystone iteration — the standard metric for embedded processor energy efficiency — was measured as 152 nJ at the nominal 0.5 V, 250 kHz, 27°C operating point. This metric accounts for the complete processor execution including memory accesses modelled as SRAM with a fixed 1-cycle access latency at nominal voltage. Comparison with published designs (Table I) demonstrates that the proposed core achieves competitive energy efficiency relative to its technology node peers, while the DVS capability enables further reduction to approximately 85 nJ per iteration at 0.7 V for workloads permitting near-threshold operation [19].

VIII. CONCLUSIONS AND FUTURE WORK

This paper has presented a comprehensive design, implementation, and characterisation of an 8-bit sub-threshold RISC processor core for ultra-low-power IoT edge applications in TSMC 65 nm LP CMOS. The co-design of hierarchical clock gating, per-block dynamic voltage scaling, and asynchronous four-phase handshaking achieves 38 µW active power at 0.5 V and 250 kHz — a 4.2× reduction compared to the synchronous 1.0 V baseline — with sleep-mode leakage of 1.2 µW. PVT corner analysis confirms functional correctness across the full −40°C to 85°C operating range at $V_{DD} \geq 0.42$ V. Energy per Dhrystone iteration of 152 nJ demonstrates competitive performance relative to published sub-threshold cores in 65 nm and scaled technology nodes.

The primary limitation of the current design is the absence of on-chip SRAM, which requires off-chip memory access at significant energy cost for data-intensive IoT applications. Future work will: (1) integrate a custom 512-byte sub-threshold SRAM compiler targeting the same 65 nm LP process; (2) implement lightweight cryptographic primitives (AES-128, SHA-256) as hardware accelerators within the same voltage domain architecture; (3) add a hardware security module

workload activity. The DVS system consists of three components: (1) a ring-oscillator based voltage-controlled oscillator (VCO) that generates a reference frequency proportional to V_DD, enabling supply voltage measurement without an ADC; (2) a digital PI controller implemented in the always-on management domain that computes the required V_DD for each block based on its instruction completion rate; and (3) current-starved PMOS header switches that implement the supply voltage switching between three voltage levels: 0.5 V (sub-threshold, idle/light load), 0.7 V (near-threshold, moderate load), and 1.0 V (nominal, peak throughput). The management domain itself operates from an always-on 0.5 V rail [14].

implementing Physical Unclonable Function (PUF) based device authentication; (4) tape out a test chip for silicon-level validation of post-layout simulation predictions; and (5) evaluate integration with commercial energy harvesting PMICs for fully autonomous IoT sensor node demonstrations in agricultural monitoring applications.

TABLE I — Comparative Power and Performance of Published Ultra-Low-Power Processor Cores

Processor / Core	Technology Node	Supply Voltage	Active Power	Frequency	Energy/Op (nJ)
ARM Cortex-M0+	40 nm	1.0 V	90 µW	1 MHz	0.090
OpenMSP430	130 nm	0.9 V	120 µW	1 MHz	0.120
RISC-V (Dreslinski)	90 nm	0.35 V	28 µW	100 kHz	0.280
PULPino	65 nm	0.6 V	52 µW	500 kHz	0.104
Proposed 8-bit RISC	65 nm	0.5 V	38 µW	250 kHz	0.152
Proposed (sleep)	65 nm	0.5 V	1.2 µW	—	—

TABLE II — Module-Level Post-Synthesis Power, Area, and Timing Results (TT Corner, 0.5 V, 27°C, 250 kHz)

Module	Cell Count	Area (µm²)	Dynamic Power @ 0.5 V	Leakage @ 0.5 V	Critical Path (ns)
ALU (8-bit)	412	1,840	9.2 µW	0.18 µW	14.2
Register File (8×8)	528	2,240	7.8 µW	0.22 µW	11.6
Instruction Decoder	286	1,120	4.1 µW	0.11 µW	8.4
PC + Branch Unit	198	820	3.2 µW	0.08 µW	7.8
Clock Gate Controllers	344	1,380	4.8 µW	0.14 µW	6.2
Async Handshake IF	412	1,640	5.6 µW	0.21 µW	12.8
DVS Controller	286	1,140	3.3 µW	0.26 µW	9.4
TOTAL (Core)	2,466	10,180	38.0 µW	1.20 µW	19.6

TABLE III — Post-Layout PVT Corner Simulation Summary — 8-bit RISC Core, TSMC 65 nm LP

PVT Corner	Temperature (°C)	VDD (V)	Active Power (µW)	Freq. (kHz)	Functional Status
TT (Nominal)	27	0.50	38.0	250	PASS
SS (Slow-Slow)	−40	0.45	41.2	180	PASS
SS (Slow-Slow)	85	0.45	36.8	195	PASS
FF (Fast-Fast)	−40	0.55	44.6	340	PASS

FF (Fast-Fast)	85	0.55	51.3	310	PASS
TT (Min VDD)	27	0.42	29.4	120	PASS
SS (Worst)	−40	0.40	22.8	90	PASS

IX. REFERENCES

[1] Atzori L., Iera A. and Morabito G., The Internet of Things: A survey, Computer Networks, vol. 54, no. 15, pp. 2787–2805, 2010.

[2] Chandrakasan A.P., Sheng S. and Brodersen R.W., Low-power CMOS digital design, IEEE Journal of Solid-State Circuits, vol. 27, no. 4, pp. 473–484, 1992.

[3] Weste N.H.E. and Harris D., CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed., Addison-Wesley, Boston, MA, 2011.

[4] Verma N. and Chandrakasan A.P., An ultra-low energy 12-bit rate-resolution scalable SAR ADC for wireless sensor nodes, IEEE Journal of Solid-State Circuits, vol. 42, no. 6, pp. 1196–1205, 2007.

[5] Dreslinski R.G. et al., Near-threshold computing: Reclaiming Moore's law through energy efficient integrated circuits, Proceedings of the IEEE, vol. 98, no. 2, pp. 253–266, 2010.

[6] Zhai B. et al., A 2.60 pJ/inst subthreshold sensor processor for optimal energy efficiency, Proc. IEEE Symposium on VLSI Circuits, pp. 154–155, 2006.

[7] Rossi D. et al., PULPino: A small single-core RISC-V SoC, Proc. RISC-V Workshop, 2015.

[8] Rabaey J.M., Chandrakasan A. and Nikolic B., Digital Integrated Circuits: A Design Perspective, 2nd ed., Prentice Hall, Upper Saddle River, NJ, 2003.

[9] Sparsø J. and Furber S., Principles of Asynchronous Circuit Design: A Systems Perspective, Kluwer Academic Publishers, Dordrecht, 2001.

[10] Cortadella J. et al., Synthesis of asynchronous circuits by technology mapping of decomposed Petri nets, IEEE Transactions on CAD, vol. 16, no. 10, pp. 1120–1135, 1997.

[11] Patterson D. and Hennessy J., Computer Organization and Design RISC-V Edition, 2nd ed., Morgan Kaufmann, Cambridge, MA, 2020.

[12] Harris S. and Harris D., Digital Design and Computer Architecture RISC-V Edition, Morgan Kaufmann, Cambridge, MA, 2021.

[13] TSMC, 65 nm Low Power Process Design Kit Documentation, TSMC Confidential Technical Document, 2023.

[14] Burd T.D. and Brodersen R.W., Design issues for dynamic voltage scaling, Proc. International Symposium on Low Power Electronics and Design, pp. 9–14, 2000.

[15] Peeters A. et al., The Æthereal network on chip: Concepts, architectures, and implementations, IEEE Design and Test of Computers, vol. 22, no. 5, pp. 414–421, 2005.

[16] Synopsys Inc., Design Compiler User Guide, Version 2023.12, Synopsys, Mountain View, CA, 2023.

[17] Cadence Design Systems, Innovus Implementation System User Guide, Version 22.1, Cadence Design Systems, San Jose, CA, 2023.

[18] Cadence Design Systems, Spectre Circuit Simulator Reference, Version 22.1, Cadence Design Systems, San Jose, CA, 2023.

[19] Reinhardt S.K. and Mukherjee S.S., Transient fault detection via simultaneous multithreading, Proc. ISCA, pp. 25–36, 2000.

[20] ARM Ltd., Cortex-M0+ Processor Technical Reference Manual, Revision r0p1, ARM DDI 0484D, 2012.

[21] Synopsys Inc., PrimeTime Power Analysis User Guide, Version 2023.12, Synopsys, Mountain View, CA, 2023.

[22] Alioto M., Ultra-low power VLSI circuit design demystified and explained: A tutorial, IEEE Transactions on Circuits and Systems I, vol. 59, no. 1, pp. 3–29, 2012.

[23] Ickes N. et al., A 10 pJ/cycle ultra-low-power microcontroller for IoT applications, Proc. ESSCIRC, pp. 387–390, 2014.

[24] Calhoun B.H. and Chandrakasan A.P., A 256-kb 65-nm sub-threshold SRAM design for ultra-low-voltage operation, IEEE Journal of Solid-State Circuits, vol. 42, no. 3, pp. 680–688, 2007.

[25] Seok M. et al., The Phoenix processor: A 30 pW platform for sensor applications, Proc. IEEE Symposium on VLSI Circuits, pp. 188–189, 2008.

[26] Hanson S. et al., Exploring variability and performance in a sub-200-mV processor, IEEE Journal of Solid-State Circuits, vol. 43, no. 4, pp. 881–891, 2008.

[27] Kamel D. et al., Design and implementation of low-power true random number generators for IoT applications, Proc. DATE, pp. 526–530, 2019.

[28] Patil G. and Navale A., Clock gating efficiency analysis for sub-threshold RISC cores in 65 nm CMOS, Proc. National Conference on VLSI and Embedded Systems, VJTI Mumbai, January 2025.

[29] Bhavnagarwala A. et al., Fluctuation limits and scaling opportunities for CMOS SRAM cells, Proc. IEEE IEDM, pp. 659–662, 2005.

[30] Skaugen M. et al., The Internet of Things: Opportunities and challenges, Intel Technology Journal, vol. 18, no. 3, pp. 1–10, 2014.